Claims

What is claimed is:

1. An inverter for providing power to a load, the inverter comprising:

a pulse start component operable to receive a first input indicative of a primary current, the pulse start component generating a first output responsive to a zero crossing of the first input;

a pulse duration component operable to receive a second input indicative of a load current and a third input indicative of a direct current (DC) input voltage, the pulse duration component being operable to generate a second output responsive to the second and third inputs;

a time delay component operable to receive the first output and the DC input voltage, the time delay component introducing a time delay to generate a delayed first output;

a logic component operable to receive the delayed first output and the second output to generate a plurality of control signals;

a plurality of switches operable to convert the DC input to the primary current in response to receiving the plurality of control signals; and

a filtering component operable to filter the primary current for generating the load current.

2. The inverter of claim 1, wherein the filtering component includes a transformer having a primary section electro-magnetically coupled to a secondary section, wherein the primary current flows through the primary section, and wherein the primary section is electrically coupled to the plurality of the switches and the secondary section is electrically coupled to the load.

3. The inverter of claim 1, wherein the load is a cold cathode fluorescent lamp (CCFL).

4. The inverter of claim 1, wherein the time delay is variable, a value of the time delay being selectable responsive to the DC input voltage.

5. The inverter of claim 4, wherein the value increases as the DC input increases.

6. The inverter of claim 1, wherein the logic component imposes the time delay to assert at least one control signal for controlling a corresponding switch following the zero crossover.

7. The inverter of claim 1, wherein the plurality of switches are configured as a full-bridge.

8. The inverter of claim 1, wherein an output of the full-bridge has a constant switching frequency caused by imposing the time delay.

9. The inverter of claim 1, wherein each control signal of the plurality of control signals controls a corresponding switch by placing the switch in an ON or OFF state, and by controlling a time period in the ON state.

10. The inverter of claim 9, wherein the time delay is imposed from the zero crossing to a change in the state of the switch.

11. The inverter of claim 9, wherein the time delay causes an adjustment of the time period in the OFF state to maintain a constant switching frequency.

12. The inverter of claim 1, wherein imposing the time delay causes a subsequent zero crossing of the first input to remain fixed relative to a previous zero crossing thereby generating a constant switching frequency.

13. A method for improving efficiency of an inverter providing power to a load, the method comprising:

receiving a direct current (DC) input;

controlling a plurality of switches to generate an alternating current (AC) output in response to the DC input;

filtering the AC output to generate a filtered AC output to power the load;

detecting a zero crossing of the AC output; and

delaying the controlling of the plurality of switches to effectively maintain a constant switching frequency of the inverter in response to a change in the DC input.

14. The method of claim 13, wherein the delaying is caused by setting a time delay, wherein the time delay has a variable time value.

15. The method of claim 14, wherein the time delay varies as a predefined function of the DC input, wherein the variable time value increases as the DC input increases.

16. The method of claim 13, wherein the controlling of the plurality of switches includes placing each switch in the plurality of switches to an ON or OFF state, and by adjusting a time period in the ON state.

17. The method of claim 16, wherein the delaying imposes a time delay measured from the zero crossing to a change in the ON or OFF state.

18. The method of claim 16, wherein the time delay causes an adjustment of the time period in the OFF state to maintain the constant switching frequency.

19. The method of claim 13, wherein imposing the time delay causes a subsequent zero crossing of the AC output to remain fixed relative to a previous zero crossing thereby generating the constant switching frequency.

20. The method of claim 19, wherein the subsequent zero crossing remaining fixed relative to the previous zero crossing generates the constant switching frequency.

21. The method of claim 13, wherein the load is a cold cathode fluorescent lamp (CCFL).

22. An information handling system (IHS) comprising:

a display device; and

an inverter operable to provide power to the display device, the inverter including:

a pulse start component operable to receive a first input indicative of a primary current, the pulse start component generating a first output responsive to a zero crossing of the first input;

a pulse duration component operable to receive a second input indicative of a display device current and a third input indicative of a direct current (DC) input voltage, the pulse duration component being operable to generate a second output responsive to the second and third inputs;

a time delay component operable to receive the first output and the DC input voltage, the time delay component introducing a time delay to generate a delayed first output;

a logic component operable to receive the delayed first output and the second output to generate a plurality of control signals;

a plurality of switches operable to convert the DC input to the primary current in response to receiving the plurality of control signals; and

a filtering component operable to filter the primary current for generating the display device current.

23. The system of claim 22, wherein the display device includes a cold cathode fluorescent lamp (CCFL).